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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,008	08/22/2003	Sung-Jae Moon	PNK-0048	8963

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CANTOR COLBURN, LLP
20 Church Street
22nd Floor
Hartford, CT 06103

EXAMINER	
NGUYEN, HOAN C	
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2871	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/646,008	MOON, SUNG-JAE	
	Examiner	Art Unit	
	HOAN C. NGUYEN	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-10,13-15,18-22 and 26-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-10,13-15,18-22 and 26-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's arguments with respect to claims 1-5, 7-10, 13-15, 18-22, and new claims 27-33 based on the Response filed on 2/26/2008 have been considered but are moot in view of the new ground(s) of rejection. Therefore, this is Final action.

Claim 6, 16-17 and 23-25 are cancelled. New claims 27-33 are added. Therefore claims 1-5, 7-10, 13-15, 18-22 and 26-33 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 1 and 14 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for transmitting signals to gate lines 121 and data lines 171, does not reasonably provide enablement for testing. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to test the invention commensurate in scope with these claims. The shorting bar 320 connects to all the first and second driving signal wires 521/522 and data leads 520; therefore the testing signals with different voltages transmitting through the first and second driving signal wires 521/522 and data leads 520 from outside will be short-circuit with a same electrical potential on the shorting bar and cannot be able to operate the LCD device since all data lines and gate lines have been short-circuit on the

shorting bar. LCD is operable if the shorting bar is cut. The operating LCD cannot include the shorting bar.

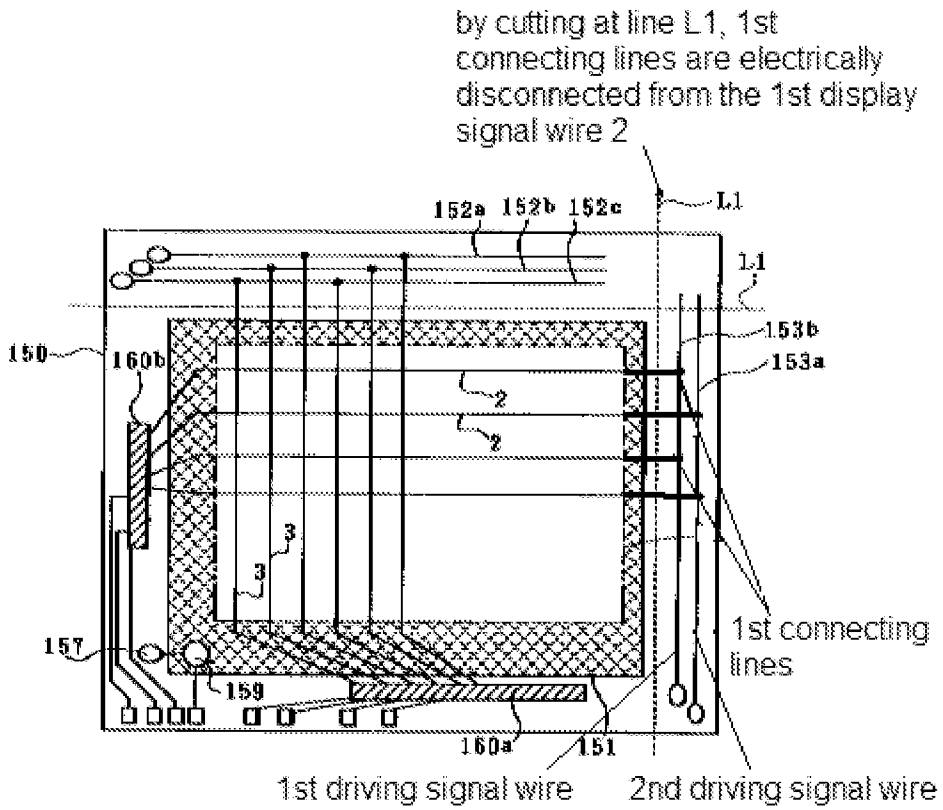
Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 7-10, 13, 15, 18-19 and 26-29 and 31-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Nagata et al. (US006172410B1).

Nagata et al. teach (Fig. 17) a liquid crystal display device comprising:



Claim 1:

- a liquid crystal panel including
  - a first display signal wire having a plurality of a first display signal lines 2,
  - a second signal wire having a plurality of a second display signal lines 3 that cross the first display signal lines,
  - a plurality of switching elements (inherence for active matrix display) each of which is connected to both of one of the first display signal lines and one of the second display signal lines, and
  - pixel electrodes inherently connected to the switching elements;

- a first driving signal wire 153b transmitting driving signals from an outside of the display panel to the first display signal lines 2, wherein the first driving signal wire is separated from the first and second display signal wires, the switching elements (inherence for active matrix display), and the pixel electrodes, and includes a first pad connected thereto at its near end;
- a plurality of first connecting lines disposed between the first driving signal wire and a part of the first display signal wire 2, and connected to at least one of the first driving signal wire and the part of the first display signal wire.

wherein the first connecting lines are electrically disconnected from the part of the first display signal wire after cutting at the cutting line L1.

Claim 7:

- a second driving signal wire 153a transmitting driving signals for the first display signal lines 2, wherein the second driving signal wire is separated from the first and second display signal wires, the switching elements, and the pixel electrodes, and includes a second pad connected thereto at its near end.

Claim 26:

- a second driving signal wire 153a transmitting driving signals from an outside of the display panel to the first display signal lines 2, wherein the second driving signal wire 153a is separated from the first and second display signal wires, the switching elements, and the pixel electrodes, and includes a second pad connected thereto at its near end.

wherein

Claim 8:

- a distance between the first driving signal wire 153b and the first display signal wire 3 is smaller than a distance between the second driving signal wire 153a and the first display signal wire 2.

Claim 9:

- a plurality of second connecting lines disposed between the second driving signal wire 153a and at least another part of the first display signal wire 2, connected to at least one of the second driving signal wire 153a and the another part of the first display signal wire 2, wherein the second connected lines are electrically disconnected from the another part of the first display signal wire 2.

Claim 10:

- the first and second connecting lines are alternately disposed.

Claim 13:

- the first connecting line is electrically connected to the first display signal wire 2 and the first driving signal wire

Claim 15:

- the first driving signal wire further comprises a plurality of second pads connected at connections thereto at its intermediate portion.

Claim 18:

- the first driving signal wire extends to an edge of the panel.

Claim 19:

- the first display signal wire 153b transmits gate signals for inherently turning on and off the switching elements, and the second display signal wire transmits data signals for the pixel electrodes applied through the switching elements.

Claim 27:

- a substrate;
- a gate driver 160a disposed on the substrate;
- a plurality of gate lines 3 electrically connected to the gate driver;
- a plurality of data lines 2 disposed substantially perpendicular to the plurality of gate lines;
- a plurality of switching elements (inherence), each switching element being connected to at least one gate line and at least one data line; and
- a plurality of pixel electrodes (inherence), each pixel electrode being connected to at least one switching element; and a first driving signal line configured to transmit driving signals from an outside of the display panel to the gate driver and also configured to transmit a first test signal via a plurality of first connecting lines to at least one of the plurality of gate lines,

wherein each first connecting line is disposed between, and connected to, the first driving signal line and at least one of the plurality of gate lines.

Claim 28:

- the gate driver is an integrated chip.

Claim 29: the plurality of first connecting lines is configured to be severable along a single linear cutting path along L1.

Claim 31:

- a second driving signal wire configured to transmit driving signals from an outside of the display panel to the gate driver and also configured to transmit a second test signal via a plurality of second connecting lines to at least one of the plurality of gate lines,

wherein each second connecting line is disposed between, and connected to, the second driving signal wire and at least one of the plurality of gate lines, the second driving signal wire is disposed between the first driving signal wire and the plurality of gate lines, and the first connecting lines are longer than the second connecting lines

Claim 32:

- a substrate;
- a gate driver disposed on the substrate
- a plurality of gate lines electrically connected to the gate driver;
- a plurality of data lines disposed substantially perpendicular to the plurality of gate lines;
- a plurality of switching elements, each switching element being connected to at least one gate line and at least one data line; and
- a plurality of pixel electrodes, each pixel electrode being connected to at least one switching element;
- a driving signal line configured to transmit driving signals from an outside of the display panel to the gate driver and also configured to transmit a test signal via a plurality of connecting lines to at least one of the plurality of gate lines,

wherein each connecting line is disposed between, and connected to, the driving signal line and the at least one of the plurality of gate lines, and the driving signal line and the connecting lines are disposed at substantially the same cross-sectional height from the substrate.

Claim 33:

- a substrate;
- a gate driver disposed on the substrate a plurality of data lines disposed substantially perpendicular to the plurality of gate lines;
- a data driver electrically connected to the plurality of data lines;
- a plurality of switching elements, each switching element being connected to at least one gate line and at least one data line; and a plurality of pixel electrodes,
- each pixel electrode being connected to at least one switching element; a driving signal line configured to transmit driving signals from an outside of the display panel to at least one of the plurality of data lines and the data driver; and
- a plurality of connecting lines, each connecting line being disposed between, and connected to, the driving signal line and at least one of the plurality of data lines.

2. Claims 1, 7-10, 13, 15, 18-21, 26-27 and 29-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishiki et al. (US6111620A).

Nishiki et al. teach (Fig. 1) a liquid crystal display device comprising:

Claim 1:

- a liquid crystal panel including

- a first display signal wire having a plurality of a first display signal lines 1a,
- a second signal wire having a plurality of a second display signal lines 2a that cross the first display signal lines,
- a plurality of switching elements TFT each of which is connected to both of one of the first display signal lines and one of the second display signal lines, and
- pixel electrodes connected to the switching elements;

- a first driving signal wire 6a transmitting driving signals from an outside of the display panel to the first display signal lines, wherein the first driving signal wire is separated from the first and second display signal wires, the switching elements, and the pixel electrodes, and includes a first pad C4 connected thereto at its near end;
- a plurality of first connecting lines 4 at disposed between the first driving signal wire and a part of the first display signal wire, and connected to at least one of the first driving signal wire and the part of the first display signal wire.

wherein the first connecting lines are electrically disconnected from the part of the first display signal wire after cutting along line 23.

Claim 7:

- a second driving signal wire 6b transmitting driving signals for the first display signal lines 21, wherein the second driving signal wire is separated from the first

and second display signal wires, the switching elements, and the pixel electrodes, and includes a second pad connected thereto at its near end.

Claim 26:

- a second driving signal wire 6b transmitting driving signals from an outside of the display panel to the first display signal lines, wherein the second driving signal wire 6b is separated from the first and second display signal wires, the switching elements, and the pixel electrodes, and includes a second pad connected thereto at its near end.

Wherein

Claims 2-4:

- a plurality of drivers respectively connected to the first driving signal wire, wherein each of the drivers is in the form of a chip and each of the drivers is formed on the liquid crystal panel.

Claim 5:

- each of the drivers is directly connected to the first driving signal wire.

Claim 8:

- a distance between the first driving signal wire 6a (inside) and the first display signal wire is smaller than a distance between the second driving signal wire 6b (outside) and the first display signal wire 21.

Claim 9:

- a plurality of second connecting lines disposed between the second driving signal wire 6b and at least another part of the first display signal wire, connected to at

least one of the second driving signal wire 6b and the another part of the first display signal wire, wherein the second connected lines are electrically disconnected from the another part of the first display signal wire.

Claim 10:

- the first and second connecting lines are alternately disposed.

Claim 13:

- the first connecting line is electrically connected to the first display signal wire and the first driving signal wire

Claim 15:

- the first driving signal wire further comprises a plurality of second pads connected at connections thereto at its intermediate portion.

Claim 18:

- the first driving signal wire extends to an edge of the panel.

Claim 19:

- the first display signal wire 6a transmits gate signals for inherently turning on and off the switching elements, and the second display signal wire transmits data signals for the pixel electrodes applied through the switching elements.

Claim 20:

- the first display signal wire 6a inherently transmits a ground voltage or power supply to IC 140.

Claims 21:

- the first display signal wire transmits data signals for the pixel electrodes, and the second display signal wire controls inherently turning on and off of the switching elements such that the transmission of the data signals to the pixel electrodes is controlled.

Claim 27:

- a substrate;
- a gate driver (driving modules installing after or before cutting shorting wires) disposed on the substrate;
- a plurality of gate lines 3 electrically connected to the gate driver;
- a plurality of data lines 2 disposed substantially perpendicular to the plurality of gate lines;
- a plurality of switching elements, each switching element being connected to at least one gate line and at least one data line; and
- a plurality of pixel electrodes, each pixel electrode being connected to at least one switching element; and a first driving signal line configured to transmit driving signals from an outside of the display panel to the gate driver and also configured to transmit a first test signal via a plurality of first connecting lines to at least one of the plurality of gate lines,

wherein each first connecting line is disposed between, and connected to, the first driving signal line and at least one of the plurality of gate lines.

Claim 29:

- the plurality of first connecting lines is configured to be severable along a single linear cutting path along L1.

Claim 30:

- a shorting bar 8 intersecting the data lines and the first driving signal line, wherein the shorting bar is configured to be removed by edge grinding along a cutting line.

Claim 31:

- a second driving signal wire 6b configured to transmit driving signals from an outside of the display panel to the gate driver and also configured to transmit a second test signal via a plurality of second connecting lines to at least one of the plurality of gate lines,

wherein each second connecting line is disposed between, and connected to, the second driving signal wire and at least one of the plurality of gate lines, the second driving signal wire is disposed between the first driving signal wire and the plurality of gate lines, and the first connecting lines are longer than the second connecting lines

Claim 32:

- a substrate;
- a gate driver (driving modules installing after or before cutting shorting wires) disposed on the substrate
- a plurality of gate lines electrically connected to the gate driver;
- a plurality of data lines disposed substantially perpendicular to the plurality of gate lines;

- a plurality of switching elements, each switching element being connected to at least one gate line and at least one data line; and
- a plurality of pixel electrodes, each pixel electrode being connected to at least one switching element;
- a driving signal line configured to transmit driving signals from an outside of the display panel to the gate driver and also configured to transmit a test signal via a plurality of connecting lines to at least one of the plurality of gate lines,

wherein each connecting line is disposed between, and connected to, the driving signal line and the at least one of the plurality of gate lines, and the driving signal line and the connecting lines are disposed at substantially the same cross-sectional height from the substrate.

Claim 33:

- a substrate;
- a gate driver (driving modules installing after or before cutting shorting wires) disposed on the substrate a plurality of data lines disposed substantially perpendicular to the plurality of gate lines;
- a data driver electrically connected to the plurality of data lines;
- a plurality of switching elements, each switching element being connected to at least one gate line and at least one data line; and a plurality of pixel electrodes,
- each pixel electrode being connected to at least one switching element; a driving signal line configured to transmit driving signals from an outside of the display panel to at least one of the plurality of data lines and the data driver; and

- a plurality of connecting lines, each connecting line being disposed between, and connected to, the driving signal line and at least one of the plurality of data lines.

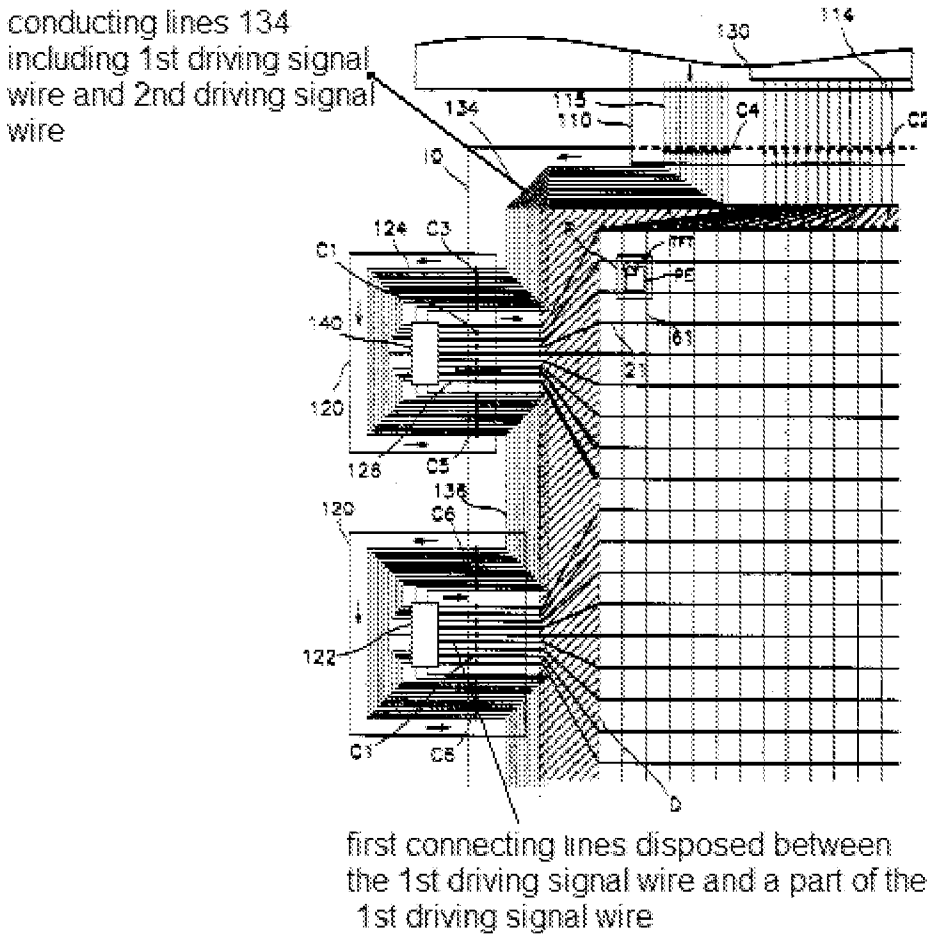
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-5, 7-10, 13, 15, 18-19, 20-22, 26-29 and 31-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US6636288B2).

Kim et al. teach (Fig. 1) a liquid crystal display device comprising:

Claim 1:

- a liquid crystal panel including
  - a first display signal wire having a plurality of a first display signal lines 21,
  - a second signal wire having a plurality of a second display signal lines 61 that cross the first display signal lines,
  - a plurality of switching elements TFT each of which is connected to both of one of the first display signal lines and one of the second display signal lines, and
  - pixel electrodes PE inherently connected to the switching elements;



- a first driving signal wire 134 transmitting driving signals from an outside of the display panel to the first display signal lines 21, wherein the first driving signal wire is separated from the first and second display signal wires, the switching elements, and the pixel electrodes, and includes a first pad C4 connected thereto at its near end;
- a plurality of first connecting lines (between the chip 120/122 and the contact C1) at disposed between the first driving signal wire and a part of the first display

signal wire 21, and connected to at least one of the first driving signal wire and the part of the first display signal wire.

wherein the first connecting lines are electrically disconnected from the part of the first display signal wire before contact at C1

Claim 7:

- a second driving signal wire transmitting driving signals 134 for the first display signal lines 21, wherein the second driving signal wire is separated from the first and second display signal wires, the switching elements, and the pixel electrodes, and includes a second pad connected thereto at its near end.

Claim 26:

- a second driving signal wire 134 transmitting driving signals from an outside of the display panel to the first display signal lines 21, wherein the second driving signal wire 134 is separated from the first and second display signal wires, the switching elements, and the pixel electrodes, and includes a second pad connected thereto at its near end.

Wherein

Claims 2-4:

- a plurality of drivers respectively connected to the first driving signal wire, wherein each of the drivers is in the form of a chip and each of the drivers is formed on the liquid crystal panel.

Claim 5:

- each of the drivers is directly connected to the first driving signal wire.

Claim 8:

- a distance between the first driving signal wire 134 (inside) and the first display signal wire 21 is smaller than a distance between the second driving signal wire 134 (outside) and the first display signal wire 21.

Claim 9:

- a plurality of second connecting lines disposed between the second driving signal wire 134 and at least another part of the first display signal wire 21, connected to at least one of the second driving signal wire 134 and the another part of the first display signal wire 21, wherein the second connected lines are electrically disconnected from the another part of the first display signal wire 21.

Claim 10:

- the first and second connecting lines are alternately disposed.

Claim 13:

- the first connecting line is electrically connected to the first display signal wire 21 and the first driving signal wire

Claim 15:

- the first driving signal wire further comprises a plurality of second pads connected at connections thereto at its intermediate portion.

Claim 18:

- the first driving signal wire extends to an edge of the panel.

Claim 19:

- the first display signal wire 134 transmits gate signals for inherently turning on and off the switching elements, and the second display signal wire transmits data signals for the pixel electrodes applied through the switching elements.

Claim 20:

- the first display signal wire 134 inherently transmits a ground voltage or power supply to IC 140.

Claims 21-22:

- the first display signal wire transmits data signals for the pixel electrodes, and the second display signal wire controls inherently turning on and off of the switching elements such that the transmission of the data signals to the pixel electrodes is controlled, wherein the first driving signal wire transmits gray voltages, a clock signal, or a driving voltage to the drivers.

Claim 27:

- a substrate;
- a gate driver 160a disposed on the substrate;
- a plurality of gate lines 3 electrically connected to the gate driver;
- a plurality of data lines 2 disposed substantially perpendicular to the plurality of gate lines;
- a plurality of switching elements (inherence), each switching element being connected to at least one gate line and at least one data line; and
- a plurality of pixel electrodes (inherence), each pixel electrode being connected to at least one switching element; and a first driving signal line configured to

transmit driving signals from an outside of the display panel to the gate driver and also configured to transmit a first test signal via a plurality of first connecting lines to at least one of the plurality of gate lines,

wherein each first connecting line is disposed between, and connected to, the first driving signal line and at least one of the plurality of gate lines.

Claim 28:

- the gate driver is an integrated chip.

Claim 29:

- the plurality of first connecting lines is configured to be severable along a single linear cutting path along L1.

Claim 31:

- a second driving signal wire configured to transmit driving signals from an outside of the display panel to the gate driver and also configured to transmit a second test signal via a plurality of second connecting lines to at least one of the plurality of gate lines,

wherein each second connecting line is disposed between, and connected to, the second driving signal wire and at least one of the plurality of gate lines, the second driving signal wire is disposed between the first driving signal wire and the plurality of gate lines, and the first connecting lines are longer than the second connecting lines

Claim 32:

- a substrate;
- a gate driver disposed on the substrate

- a plurality of gate lines electrically connected to the gate driver;
- a plurality of data lines disposed substantially perpendicular to the plurality of gate lines;
- a plurality of switching elements, each switching element being connected to at least one gate line and at least one data line; and
- a plurality of pixel electrodes, each pixel electrode being connected to at least one switching element;
- a driving signal line configured to transmit driving signals from an outside of the display panel to the gate driver and also configured to transmit a test signal via a plurality of connecting lines to at least one of the plurality of gate lines,

wherein each connecting line is disposed between, and connected to, the driving signal line and the at least one of the plurality of gate lines, and the driving signal line and the connecting lines are disposed at substantially the same cross-sectional height from the substrate.

Claim 33:

- a substrate;
- a gate driver disposed on the substrate a plurality of data lines disposed substantially perpendicular to the plurality of gate lines;
- a data driver electrically connected to the plurality of data lines;
- a plurality of switching elements, each switching element being connected to at least one gate line and at least one data line; and a plurality of pixel electrodes,

- each pixel electrode being connected to at least one switching element; a driving signal line configured to transmit driving signals from an outside of the display panel to at least one of the plurality of data lines and the data driver; and
- a plurality of connecting lines, each connecting line being disposed between, and connected to, the driving signal line and at least one of the plurality of data lines.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata et al. (US006172410B1 as applied to claims in view of Nishiki et al. (US6111620A).

Nagata et al. fail to disclose a liquid crystal display device comprising a shorting bar intersecting the data lines and the first driving signal line, wherein the shorting bar is configured to be removed by edge grinding along a cutting line.

Nishiki et al. teach (Fig. 1) a liquid crystal display device comprising a shorting bar intersecting the data lines and the first driving signal line, wherein the shorting bar 8 is configured to be removed by edge grinding along a cutting line for detecting leakage defects among the gate wires and those among the data wires, correct the revealed defects, and confirm the corrections easier at a low cost.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as Makinouchi disclosed with a shorting bar intersecting the data lines and the first driving signal line, wherein the shorting bar 8 is configured to be removed by edge grinding along a cutting line for detecting leakage defects among the gate wires and those among the data wires, correct the revealed defects, and confirm the corrections easier at a low cost. (abstract) as Nishiki et al. taught.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN C. NGUYEN whose telephone number is (571) 272-2296. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HOAN C. NGUYEN
Examiner
Art Unit 2871

Chn

/David Nelms/
Supervisory Patent Examiner, Art Unit 2871